Appl. No. 09/816,926
Letter Dated October 19, 2004
Reply to Notice of Non-Compliant Amendment of October 13, 2004

CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). ~~In a~~ A configurable hardware block, comprising: ~~of the type which, depending on its configuration, is enabled~~

a universal configurable unit being selectively configured to read data stored in a memory unit, to process the data in at least one of arithmetic and logical processing units, and to write data representing a result of the processing to the memory unit, ~~the improvement which comprises the hardware block is~~ said universal configurable unit having an asynchronous combinational circuit to ~~asynchronously link components of said universal~~ configurable unit, and said universal configurable unit being capable of interacting autonomously with external hardware.

Claim 2 (original). The configurable hardware block according to claim 1, wherein the hardware block is configured for interaction with the external hardware

comprising instructing the memory unit to accept data supplied by the external hardware in response to specific events.

Claim 3 (original). The configurable hardware block according to claim 1, wherein the hardware block is configured for interaction with the external hardware comprising outputting one of data and signals to the external hardware.

Claim 4 (original). The configurable hardware block according to claim 1, wherein the external hardware is selected from the group consisting of other configurable hardware blocks, a control unit operating in parallel or at a supervisory level, and other components of a system containing the configurable hardware block.

Claim 5 (original). The configurable hardware block according to claim 4, wherein the data and/or signals output to the external hardware are used to signal specific states or events.

Claim 6 (original). The configurable hardware block according to claim 1, which comprises a timer generation unit generating a clock signal for the memory unit.

Claim 7 (original). The configurable hardware block according to claim 6, wherein said timer generation unit is configured to generate the clock signal depending on one or more periodic or non-periodic signals originating at least to some extent from the external hardware.

Claim 8 (original). The configurable hardware block according to claim 1, which comprises a signaling unit configured to generate report signals for the external hardware.

Claim 9 (original). The configurable hardware block according to claim 8, wherein the report signals signal an occurrence of predefined states and/or events in the configurable hardware block.

Claim 10 (original). The configurable hardware block according to claim 8, wherein said signaling unit is configured to generate a report signal signaling that an operation or sequence of operations to be executed repeatedly in the hardware block has been executed a specified number of times.

Claim 11 (original). The configurable hardware block according to claim 8, wherein the signaling unit is configured to generate a report signal useable as an interrupt request for a program-controlled unit.

Claim 12 (original). The configurable hardware block according to claim 8, which comprises at least one comparison unit generating and outputting a report signal.

Claim 13 (original). The configurable hardware block according to claim 12, wherein at least some of said comparison units are configurable comparison units configured to subject incoming signals to operations selected from the group consisting of selectable compare operations, checks for TRUE, and checks for UNTRUE.

Claim 14 (original). The configurable hardware block according to claim 13, wherein the selectable compare operations are selected from the group of compare operations consisting of greater than, greater than or equal to, not equal to, smaller than, and smaller than or equal to comparisons.

Claim 15 (currently amended). The configurable hardware block according to claim 12, wherein at least some of said

comparison units have a multiplexer connected in series ~~series-connected~~ on an input side thereof, said multiplexer determining which signals are supplied to said comparison unit as input signals.

Claim 16 (original). The configurable hardware block according to claim 1, which comprises a plurality of configurable units selected from the group consisting of sub-units selectively configurable to a required function, configurable data paths, and configurable signal paths.

Claim 17 (original). The configurable hardware block according to claim 16, wherein configurable data and signal paths to the external hardware exist or can be established.

Claim 18 (original). The configurable hardware block according to claim 1, wherein the memory unit is a register block containing a plurality of registers.

Claim 19 (original). The configurable hardware block according to claim 1, configurable on a basis of instructions or instruction sequences, and configurable to execute operations or operation sequences specified by the instructions or instruction sequences.

Claim 20 (original). The configurable hardware block according to claim 19, dimensioned to be configurable by hyperblock.

Claim 21 (original). The configurable hardware block according to claim 1, constructed and configurable to be used to replace a specific circuit.

Claim 22 (original). The configurable hardware block according to claim 1, constructed and configurable to be used to replace various specific circuits.

Claim 23 (original). The configurable hardware block according to claim 21, configured to test an integrated circuit containing the hardware block.

Claim 24 (original). The configurable hardware block according to claim 21, wherein the hardware block is configurable for use in applications selected from the group consisting of cryptography and identification applications.

Claim 25 (original). The configurable hardware block according to claim 1, which comprises a memory unit for storing interim results.